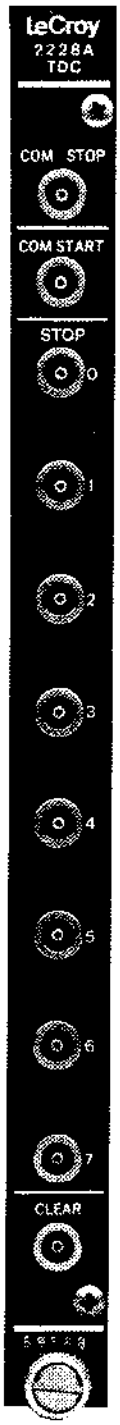
TECHNICAL DATA

LeCroy



CAMAC Model 2228A
Octal Time-to-Digital Converter

- **8 channels in single-width module**
- **11-bit resolution**
- **Switch-selectable 100, 200, and 500 nsec full-scale time ranges**
- **Time resolutions of 50, 100, or 250 psec/count**
- **Rejects stops before starts**
- **Fast clear input**
- **Internal test capability**
- **Common stop input for precision on-line testing**
- **Full LAM functions**
- **Fast digitizing time**
- **Q and LAM suppression**

The LeCroy Model 2228A is an Octal Time-To-Digital Converter, packaged in a No. 1 CAMAC module. It incorporates all the advanced operating characteristics which experience has indicated necessary for accurate and reliable measurement of nanosecond time intervals.

The Model 2228A has 8 independent channels, each of which measures the time from the leading edge of a common start pulse to the leading edge of its individual stop pulse. Each 2228A channel disregards any stop pulses received before a start signal and will accept only one stop for every start.

Conversion begins upon receipt of the start signal and proceeds until one of the following: a stop signal is received; the cycle is terminated by the application of a front-panel clear signal; or the TDC reaches full scale.

The 2228A converts the measured time intervals into a 11-bit digital number at the rate of 20 MHz, for a full scale digitizing time of 100 microseconds. Rear-panel control of full-scale and conversion slope permits digitization to fewer bits and a shorter conversion time if desired. The conversion clock is started in phase with the TDC start signal to assure synchronization and eliminate the inaccuarcy introduced by the free-running oscillators in conventional designs. LAM, if enabled, is generated at the end of the conversion interval.

The 2228A has three switch-selectable full-scale time ranges, 100, 200 and 500 nsec, which are digitized to 95% of 11 bits (2048 channels) and provide 50, 100, and 250 psec resolutions respectively. Longer time ranges (up to 10 microseconds) may be provided on request at slight expense of stability and accuracy.

On line testing is facilitated by either a front-panel common stop input of F(25). A signal at the common stop input generates simultaneous stops for each channel, permitting accurate testing of both front end and scaler section of the module and uniform system testing and time calibration. F(25) is provided for a quick test of the front end and scaler sections with a time measurement of 80% of full scale.

In higher rate or colliding beam experiments, excessive system deadtime due to false starts may be eliminated through use of the 2228A's fast clear input. Accepting NIM level signals, this input allows the TDC to be cleared at any point in its conversion cycle without the necessity for any Dataway operations.

All standard LAM functions are available in the 2228A to facilitate data readout. To minimize readout time, both Q and LAM may be suppressed if the module does not contain data.

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Innovators in Instrumentation

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SPECIFICATIONS
CAMAC Model 2228A
OCTAL TIME-TO-DIGITAL CONVERTER

Stop Inputs:	8, one per channel, 50 Ω impedance; Lemo-type connectors; direct-coupled; input amplitude > −450 mV; ineffective unless preceded by a "Start" input.
Common Start Input:	One, common to all channels, 50 Ω impedance; Lemo-type connector; input amplitude > −450 mV.
Common Stop Input:	One, common to all channels, 50 Ω impedance; Lemo-type connector;> −450 mV; functions identical to individual "Stop Inputs" above; used for on-line testing.
Fast Clear	One input, common to all channels; Lemo-type connector; 50 Ω impedance; −450 mV or greater clears; minimum duration 50 nsec. Requires 1.4 μsec after start of clear signal to settle to 1±1 counts. (However, if the unit is always cleared at a fixed time before each start, it will settle to a constant offset with a small uncertainty, effectively permitting fast reset times on the order of 500 nsec.)
Full-Scale Time Range:	11-bit binary output corresponds to 100, 200, and 500 nsec nominal, switch-selectable (with longest range field-adjustable up to 1 μsec). Larger full-scales possible by factory option up to 10 μsec. Both the full-scale value and conversion slope are rear-panel adjustable, permitting faster conversion at the expense of range.
Integral Non-linearity:	± 2 counts (20 nsec to full scale).
Differential Non-linearity:	Channel widths vary by ±10% (10 nsec to full scale).
Time Resolution:	50 psec on 100 nsec range; 100 psec on 200 nsec range; 250 psec on 500 nsec range.
Temperature Coefficient:	Typically (±0.02% of full scale ±0.01% of reading) per degree C.
Digitizing Time:	CAMAC modes conversion is initiated by receipt of "Start" input. Approximately 100 μsec for 11 bits; rear-panel adjustable for fewer bits, shorter conversion time.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitizing is complete.
Test Functions:	An internal start/stop is generated by F(25) with approximately 80% of full scale spacing. On-line testing and calibrations can be done with common start and common stop above.
Data:	The proper CAMAC function and address command gates the binary data of the selected channel onto the R(1) to R(11) (2^0 to 2^{10}) Dataway bus lines. The full-scale number of bits, and thus the conversion time, can be selected by a rear-panel pot and test point. (Conversion curve provided with unit.) The overflow flag is always presented on R(12).
CAMAC Commands:	Z or C: All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2". I: "Start" input is inhibited during CAMAC "inhibit" command. Q: A Q=1 response is generated in recognition of an F0 or F2 Read function, or an F8 function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules is suppressed (see Q and LAM suppression). X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: Look-At-Me signal is generated from end of digitizing until a module Clear or Clear LAM. LAM is disabled for duration of N, can be permanently enabled or disabled by the Enable or Disable function command, and can be tested by Test LAM. Switch-selectable option causes LAM to be suppressed by empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A. A(0) through A(7) are used for channel address. F(2): Read registers and clear module; requires N, A, and S2. Clears on A(7) only. F(8): Test Look-At-Me; requires LAM, N and any A from A(0) to A(7). Q is Generated if LAM is present and enabled. F(9): Clear module (and LAM); requires N and any A from A(0) to A(7), and S2. F(10): Clear Look-At-Me; requires N, S2 and any A from A(0) to A(7). F(24): Disable Look-At-Me; requires N, S2 and any A from A(0) to A(7). F(25): Test module; requires N, S2 and any A from A(0) to A(7). F(26): Enable Look-At-Me; requires N, S2 and any A from A(0) to A(7). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The Q and LAM suppress features can be disabled with side-panel switches.
Packaging:	In conformance with CAMAC standard for nuclear modules. (ESONE Report EUR4100 or IEEE Report #583.) RF-shielded CAMAC #1 module.
Power Requirements:	+24V at 25 mA; −24V at 140 mA; +6V at 600 mA; −6V at 550 mA.

SPECIFICATIONS SUBJECT TO CHANGE.